WHAT IS CLAIMED IS:

1. A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming an oxide layer overlying the substrate;

forming a buffer layer overlying the oxide layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region.

2. The method of claim 1 wherein the channel region is about 1 micron and less.

3. The method of claim 1 wherein the ferroelectric material is a PZT bearing compound.

4. The method of claim 1 wherein the buffer layer is a magnesium bearing compound.

5. The method of claim 1 wherein the buffer layer is a magnesium oxide layer, the magnesium oxide layer being a barrier layer.

6. The method of claim 1 wherein the ferroelectric material has a thickness of less than about 1,000 Angstroms.

7. The method of claim 1 wherein the buffer layer has a thickness ranging from about 7 to 100 nanometers.

8. The method of claim 1 wherein the ferroelectric material has a thickness of about 100 Angstroms and greater.

9. The method of claim 1 wherein the ferroelectric material is PZT.

10. The method of claim 1 wherein the buffer layer is a barrier diffusion layer, the barrier diffusion layer substantially preventing diffusion between the ferroelectric material to the substrate.

11. The method of claim 1 wherein the buffer material is sputtered from a substantially pure magnesium target to form a magnesium oxide layer.

12. The method of claim 11 wherein the sputtering is maintained at a temperature greater than about 400 degrees Celsius or greater than about 500 degrees Celsius.

13. The method of claim 1 wherein the buffer layer is thermally annealed.

14. The method of claim 1 wherein the ferroelectric material is highly oriented.

15. The method of claim 14 wherein the highly oriented material is a polycrystalline film.

16. The method of claim 1 wherein the ferroelectric film is substantially free from an amorphous structure.

17. The method of claim 15 wherein the polycrystalline film has a crystal structure of 100 angstroms and greater.

18. The method of claim 1 wherein buffer layer is a template to provide an oriented growth of the ferroelectric film.

19. The method of claim 1 wherein the oxide is provided by a dry oxidation process comprising an oxygen bearing compound.

20. The method of claim 1 wherein the oxide passivates the surface of the substrate to protect the channel region.

21. A method for fabricating a non-volatile memory device, the method comprising:

providing a substrate;

forming a first buffer layer overlying the substrate;

forming a second buffer layer overlying the first buffer layer;

forming a ferroelectric material overlying the substrate;

forming a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

forming first and second doped regions adjacent to first and second ends of the channel region.

22. The method of claim 21, wherein the first buffer layer is a gate oxide layer, and the second buffer layer is a MgO layer.

23. The method of claim 21, wherein the first buffer layer is an amorphous layer, and the second buffer layer is a highly-oriented layer.

24. The method of claim 23, wherein the second buffer layer has a thickness of no more than 10 nm.

25. A memory structure for integrated circuit devices, the structure comprising:

a substrate;

an oxide layer overlying the substrate;

a buffer layer overlying the oxide layer;

a ferroelectric material overlying the substrate;

a gate layer overlying the ferroelectric material, the gate layer overlying a channel region; and

a first source/drain region adjacent to a first side of the channel region and a second source/drain region adjacent to a second side of the channel region.